ABSTRACT OF THE DISCLOSURE

A system for designing connecting terminals of a semiconductor device, having a power supply cell arranging unit configured to arrange power supply cells at some of I/O slots formed in a semiconductor chip, an I/O signal cell arranging unit configured to arrange I/O signal cells at some of the I/O slots where the power supply cells are not arranged, a first connecting net generator configured to generate a first connecting net connecting the I/O slots to bumps formed on the semiconductor chip, a second connecting net generator configured to generate a second connecting net connecting the bumps to external electrodes formed on a package base, and a verifier configured to verify whether the power supply cells, I/O signal cells, and first and second connecting nets violate predetermined design rules.